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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,226	12/19/2003	Kris W. Johnson	08350.3501	8495

58982 7590 05/30/2007

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

MAIL DATE	DELIVERY MODE
05/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/739,226	JOHNSON ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/19/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 10-11, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al., Patent No. 7,010,704.

With respect to claim 1, Yang discloses a current monitoring and interrupting circuit [Fig. 2], comprising an electrically conductive line [Fig. 2; line coming out from rectifier 108, which changes AC to DC] carrying a DC current; a sensor [Fig. 2, 102; col. 7 lines 39-44, lines 50-53] that outputs a voltage level [Fig. 2; the voltage level going into node 2 of the comparator 106; col. 7 lines] indicative of a magnitude of the DC current; a comparator [Fig. 2, 106] that compares the voltage level to a reference potential [Fig. 2; two resistors R3 and R4 make up a reference potential or voltage divider; col. 7 lines 54-56] and generates a circuit indicator signal [Fig. 2; signal coming out from the comparator 106]; and a logic-based current interrupter [Fig. 2; 110] that controls the current in the line in response to the circuit indicator signal [col. 5 lines 28-35].

With respect to claim 10, Yang discloses that the logic-based current interrupter [Fig. 2, 110] includes a Boolean logic device [Fig. 2; it is a D type flip-flop].

With respect to claim 11, Yang discloses that the Boolean logic device includes a flip-flop [Fig. 2; 110; col. 8 lines 35-40].

With respect to claim 14, Yang discloses a method of monitoring and interrupting DC current [Fig. 2] flowing in an electrically conductive line [Fig. 2; line coming out from rectifier 108, which changes AC to DC], comprising sensing the DC current flowing in the electrically conductive line [Fig. 2; the DC current flowing through R1 is sensed in the electrically conductive line coming out from rectifier 108]; generating a voltage level indicative of a magnitude of the DC current [Fig. 2; resistors R1 and R2 generate a voltage level indicative of a magnitude of the DC current]; comparing the voltage level to a reference voltage [Fig. 2; two resistors R3 and R4 make up a reference potential or voltage divider; col. 7 lines 54-56] and generating a circuit indicator signal [Fig. 2; signal coming out from the comparator 106]; and using a logic-based device [Fig. 2; 110] to cause an interruption of the DC current flowing in the electrically conductive line if the circuit indicator signal is indicative of a condition where the voltage level is higher than the reference voltage [col. 5 lines 28-35].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 12-13, 15-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., Patent No. 7,010,704, in view of Canova et al., Publication No. US 2003/0202304.

Yang does not disclose a current switch disposed in the electrically conductive line and connected to the logic-based interrupter.

With respect to claim 2, Conova discloses a current switch [Fig. 1, 7] disposed in the electrically conductive line and connected to the logic-based signal [Fig. 1, 13; most microprocessor would have logic-based controller in it].

Yang and Canova are analogous current monitoring and interrupting circuits connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Canova, which teaches a switch, with the circuit of Yang, for the benefit of interrupting electric power supply to a user circuit when the current exceeds a pre-set value.

With respect to claim 3, Canova teaches that the current switch [Fig. 1, 7] includes a MOSFET [Page 2, paragraph 0020, lines 17-19].

With respect to claim 4, Canova further includes a fuse [Fig. 1, 5, Page 1, paragraph 0020, lines 4-5, lines 3-7].

With respect to claim 12, Canova further includes a reset circuit [Page 1, paragraph 0012, lines 8-10, the microprocessor 13 in Fig. 1 comprises a reset circuit, which sends a reset signal to the circuit breaker].

With respect to claim 13, Canova further includes an indicator [Fig. 1, 3] that signals whether the current is flowing in the electrically conductive line [Page 1, paragraph 0020, lines 4-8; the block 3 in Fig. 1 comprises a current-read resistor, which sends a signal to voltage comparator].

With respect to claim 15, Canova discloses that the logic-based device [Fig. 1, most microprocessor would have logic-based controller in it] includes a flip flop that controls a current switch [Fig. 1, 7]

With respect to claim 16, Canova teaches that the current switch includes a MOSFET [Page 2, paragraph 0020, lines17-19].

With respect to claim 17, Canova further includes resetting the circuit breaker [Fig. 1, 7] to restore the current flowing in the electrically conductive line [Canova does not disclose a logic-based device as an interrupter (or circuit breaker), but Parker teaches a trip latch 57 as a logic-based device]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Parker into Canova, to reset the trip latch 57 once the cause of the tripping has been determined.

With respect to claim 18, Canova teaches that the step of resetting is performed automatically [Page 1, paragraph 0012, lines 8-10; the microprocessor 13 is programmed to reset the circuit breaker automatically].

With respect to claim 19, Canova further includes generating an indicator signal [Fig. 1, 3] that conveys whether the current is flowing in the electrically conductive line [Page 1, paragraph 0020, lines 4-8; the block 3 in Fig. 1 comprises a current-read resistor, which sends a signal to voltage comparator].

With respect to claim 21, Yang discloses a circuit breaker [Fig. 2] for interrupting a flow of DC current in an electrically conductive line, comprising a sensor [Fig. 2, 102; col. 7 lines 39-44, lines 50-53] that outputs a voltage level indicating of a magnitude of the DC current [Fig. 2; resistors R1 and R2 generate a voltage level indicative of a magnitude of the DC current]; a comparator [Fig. 2, 106] that compares the voltage level to a reference potential and generates a circuit indicator signal [Fig. 2; two resistors R3 and R4 make up a reference potential or voltage divider; col. 7 lines 54-56]; a logic device [Fig. 2; 110] that receives the circuit indicator signal and generates a current interrupt signal when the circuit indicator signal corresponds to a condition where the voltage level is greater than the reference potential [col. 5 lines 28-35]. However, Yang does not disclose a current switch.

Canova discloses a current switch [Fig. 1, 7] that selectively prevents the flow of current in the electrically conductive line in response to the current interrupt signal [Page 2, paragraph 0020, lines17-19].

Yang and Canova are analogous current monitoring and interrupting circuits connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine

the teachings of Canova, which teaches a switch, with the circuit of Yang, for the benefit of interrupting electric power supply to a user circuit when the current exceeds a pre-set value.

Claims 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., Patent No. 7,010,704, in view of Huang et al., Patent No. 6,952,335.

Yang discloses an electrically conductive line, but does not disclose that the electrically conductive line is part of an electrical bus energized to at least 60 VDC. Huang teaches a solid-state DC circuit breaker.

With respects to claims 5-7, Huang teaches that the electrically conductive line is part of an electrical bus energized to at least 60, 200 and 300 VDC. [Abstract, liens 1-2, Col. 3, lines 56-57, The DC circuit breaker is capable of interrupting high DC currents, which means the circuit breaker is connected across a high voltage source, which can include 60 VDC, 200 VDC, and 300 VDC].

Yang and Huang are analogous monitoring and interrupting circuits connected between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Huang, which teaches high voltage sources, with the circuit of Yang, for the benefit of providing a circuit breaker that is capable of interrupting high DC currents, which come from high DC voltages.

With respect to claim 9, Huang teaches that the sensor includes a Hall effect device [Col. 4, lines 62-67].

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., Patent No. 7,010,704, in view of Yoshida et al., Patent No. 6,791,207.

Yang discloses an electrically conductive line connected to a circuit breaker, and then to the load, but does not disclose that the electrically conductive line is part of a vehicular electrical bus. Yoshida teaches an apparatus for supplying power from a power supply to plural electric loads mounted on an automobile.

With respect to claim 8, Yoshida discloses that the electrically conductive line is a part of a vehicular electrical bus [Col. 2, lines 18-23].

Yang and Yoshida are analogous monitoring and interrupting circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Yoshida, with the circuit of Yang, for the benefit of having double protection or even triple protection against short circuit in an automobile.

Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang, in view of Canova, as applied to claim 21 above, and further in view of Huang et al., Patent No. 6,952,335.

Yang and Canova both disclose current sensors, but do not disclose that the sensor includes a Hall effect current transducer.

With respect to claim 22, Huang teaches that the sensor includes a Hall effect current transducer [Col. 4, lines 62-67].

All three teachings are analogous current sensors between power supply and loads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have Huang's Hall effect current transducer, with Yang's circuit, for the benefit of having the sensor located in the load side.

With respect to claim 23, Yang discloses that the logic device includes a flip-flop [Fig. 2; 110; col. 8 lines 35-40].

With respect to claim 24, Canova discloses that the current switch includes a MOSFET [Page 2, paragraph 0020, lines 17-19].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 7:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

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DHP
05/17/2007

Stephen W Jackson
5-18-07

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